Introduction

• Backend technology: fabrication of interconnects and the dielectrics that electrically and physically separate them.

• Early structures were very simple by today's standards.

• More metal interconnect levels increases circuit functionality and speed.

• Local interconnects (polysilicon, silicides, TiN) versus global interconnects (usually Al).
• Backend processing is becoming more important.
  • Larger fraction of total structure and processing.
  • Starting to dominate total speed of circuit.

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• The speed limitations of interconnects can be estimated fairly simply.

\[
\tau_L = 0.89RC = 0.89 \cdot K_1 K_{ox} \varepsilon_0 \rho L^2 \left( \frac{1}{Hx_{ox}} + \frac{1}{WL_S} \right)
\]  

(1)

where \( K_{ox} \) is the dielectric constant of the oxide, \( K_1 \) accounts for fringing fields and \( \rho \) is the resistivity of the interconnect line.

• Interconnect and gate time delay versus chip area.
Historical Development and Basic Concepts

A. Contacts

• Early structures were simple Al/Si contacts.

• Highly doped silicon regions are necessary to insure ohmic, low resistance contacts.

\[ \rho_c = \rho_{co} \exp \left( \frac{2\phi_B \sqrt{m^* \varepsilon_s}}{h \sqrt{N_D}} \right) \]  \hspace{1cm} (2)

• Tunneling current through a Schottky barrier depends on the width of the barrier and hence \( N_D \).

• In practice, \( N_D, N_A > 10^{20} \) are required.

• Another practical issue is that Si is soluble in Al (\( \approx 0.5\% \) at 450°C). This can lead to "spiking" problems.

• Si diffuses into Al, voids form, Al fills voids \( \Rightarrow \) shorts!
• 1<sup>st</sup> solution - add 1-2% Si in Al to satisfy solubility. Widely used, but Si can precipitate when cooling down and increase $\rho_c$.

• Better solution: use barrier layer(s). Ti or TiSi<sub>2</sub> for good contact and adhesion, TiN for barrier.

![Diagram of interconnects and vias](image)

• See Table 11.3 in text for various barrier options.

**B. Interconnects And Vias**

• Al has been the dominant material for interconnects.
  - low resistivity
  - adheres well to Si and SiO<sub>2</sub>
  - can reduce other oxides
  - can be etched and deposited using reasonable techniques

• Problems: relatively low melting point and soft.
  - need a higher melting point material for gate electrode and local interconnect $\Rightarrow$ polysilicon.
  - hillocks and voids easily formed in Al.

• Hillocks and voids form because of stress and diffusion in Al films. Heating places Al under compression causing hillocks. Cooling back down can place Al under tension $\Rightarrow$ voids.
• Adding few % Cu stabilizes grain boundaries and minimizes hillock formation.

• A related problem with Al interconnects is “electromigration.” High current density (0.1-0.5 MA/cm²) causes movement of Al atoms in direction of electron flow.

• Can cause hillocks and voids, leading to shorts or opens in the circuit.

• Adding Cu (0.5-4 weight %) can also inhibit electromigration.

• Thus Al is commonly deposited with 1-2 wt % Si and 0.5-4 wt % Cu.
• Next development was use of other materials with lower resistivity as local interconnects, like TiN and silicides.

![Diagram of TiN and Si interconnects]

• Silicides used to 1. strap polysilicon, 2. strap junctions, 3. as a local interconnect.

• Self-aligned silicide (“salicide”) process:

![Diagram of salicide process]

• Also, recall TiN, TiSi₂ simultaneous formation in CMOS process in Chapter 2.
Multilevel metal interconnects posed new challenges.


These issues get worse with additional levels of interconnect and required a change in structure.

\[
DOP = 1 - \frac{x_{\text{step}}^f}{x_{\text{step}}^i} \tag{3}
\]
• One early approach to planarization incorporated W plugs and a simple etchback process. (Damascene process.)

• SPEEDIE simulation shows how planarization can be accomplished by overfilling the via.

• Finally, interconnects have also become multilayer structures.
• Shunting the Al helps mitigate electromigration and can provide mechanical strength, better adhesion and barriers in multi-level structures. TiN on top also acts as antireflection coating for lithography.

• Typical modern interconnect structure incorporating all these new features.

C. Dielectrics

• Dielectrics electrically and physically separate interconnects from each other and from active regions.

• Two types:
  - First level dielectric
  - Intermetal dielectric (IMD)
• **First level dielectric** is usually SiO$_2$ “doped” with P or B or both (2-8 wt. %) to enhance reflow properties.
  - PSG: phosphosilicate glass, reflows at 950-1100°C
  - BPSG: borophosphosilicate glass, reflows at 800°C.

• SEM image of BPSG oxide layer after 800°C reflow step, showing smooth topography over step.

• Undoped SiO$_2$ often used above and below PSG or BPSG to prevent corrosion of Al.

• **Intermetal dielectrics** also made primarily of SiO$_2$ today, but cannot do reflow or densification anneals because of T limitations.
• Two common problems occur, cusping and voids, which can be minimized using appropriate deposition techniques (Chapter 9).

![Diagram showing cusping and planarization](image)

• SPEEDIE simulations of silicon dioxide depositions over a step for silane deposition ($S_c = 0.4$) and TEOS deposition ($S_c = 0.1$) showing less cusping in the latter case.

![Graph showing oxide depositions](image)

• However planarization is also usually required today.
• One simple process involves planarizing with photoresist and then etching back with no selectivity.

• Spin-on-glass (SOG) is another option:
  • Fills like liquid photoresist, but becomes SiO$_2$ after bake and cure.
  • Done with or without etchback (with etchback to prevent poisoned via - no SOG contact with metal).
  • Can also use low-K SOD’s. (spin-on-dielectrics)
  • SOG oxides not as good quality as thermal or CVD oxides
  • Use sandwich layers.

• A final deposition option is HDPCVD (see chapter 9) which provides angle dependent sputtering during deposition which helps to planarize.

• The most common solution today is CMP which works very well.
• CMP is generally much better at global planarization than the etchback techniques.
• Shown below is a schematic diagram of a backend structure showing one possible dielectric multi-structure scheme. Other variations include HDP oxide or the use of CMP.

With PECVD oxide/PECVD nitride passivation bilayer on top of final metal level

• Shown above are two current backend structures from VLSI Technology, Inc. Left: three metal levels and encapsulated BPSG for the first level dielectric; SOG (encapsulated top and bottom with PECVD oxide) and CMP in the intermetal dielectrics. The multilayer metal layers and W plugs are also clearly seen. Right: five metal levels, HDP oxide (with PECVD oxide on top) and CMP in the intermetal dielectrics.
Models and Simulation

• Backend process simulation obviously relies heavily on the deposition and etching simulation tools discussed in Chapters 9 and 10.

• We will briefly consider here one additional simulation tool which is useful - reflow.

• See Chapter 11 for a discussion of other models - silicide formation, CMP, grain growth, electromigration etc.

• Reflow occurs to minimize the total energy of the system. In this case, the surface energy of the structure is reduced by minimizing the curvature.

• Surface diffusion is one reflow mechanism (metals at high T).

• Atoms will move to regions of lower chemical potential, $\mu$, which is a function of the curvature.

\[
\text{Force} = -\frac{\partial \mu}{\partial s} = -\gamma_s \Omega \frac{\partial K}{\partial s}
\]

(4)

where force is on the atom, $\gamma_s$ is the per-area surface energy, $\Omega$ is the atomic volume of the atom, $K$ is the curvature, and $s$ is the length along the surface.

The curvature, $K$, is equal to the inverse of the radius of curvature, $R$, at that point:

\[
K = \frac{1}{R}
\]

(5)
The force acting upon an atom is in the direction away from a point of higher curvature to a point of lower curvature. A smoothing of the topography results.

The surface flux of atoms, $F_S$ then equals:

$$F_S = -\frac{D_S \gamma_s \Omega \nu}{kT} \frac{\partial K}{\partial s}$$

where $\nu$ is the number of atoms per unit area, and $D_S$ is the surface diffusivity of the atoms.
• Simulations of R. Brain, for reflow of Cu at 800K for different trench sizes: a. 1 x 1 μm; b. 0.5 x 1 μm; c. 0.33 x 1 μm; and d. three 0.5 x 1 μm trenches spaced 0.5 μm apart. (parameters given in Table 11.8 in text.)

• Note filling of trenches and smoothing of topography.

THE FUTURE OF BACKEND TECHNOLOGY

• Remember:

\[
\tau_L = 0.89RC = 0.89 \cdot K_I K_{ox} \varepsilon_{o} \rho L^2 \left( \frac{1}{H_{xox}} + \frac{1}{W_{LS}} \right) \tag{1}
\]

• Need to reduce circuit delay due to interconnects.

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• Reduce metal resistivity - use Cu instead of Al.

• Aspect ratio - advanced deposition, etching and planarization methods.

• Reduce dielectric constant - use low-K materials.

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<th>Deposition technique</th>
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| Inorganic                 | SiO₂ (including PSG and BPSG)         | 3.9-5.0             | CVD
|                           |                                       |                     | Thermal oxidation              |
|                           |                                       |                     | Bias-sputtering                 |
|                           |                                       |                     | High density plasma             |
|                           | Spin-on-glass (SiO₂) (including PSG and BPSG) | 3.9-5.0             | SOD                            |
|                           | Modified SiO₂ (e.g. fluorinated SiO₂ or hydrogen silsesquioxane - HSQ) | 2.8-3.8             | CVD/SOD                        |
|                           | BN (Si)                               | >2.9                | CVD                            |
|                           | Si₃N₄ (only used in multilayer structure) | 5.8-6.1             | CVD                            |
| Organic                   | Polymides                             | 2.9-3.9             | SOD/CVD                        |
|                           | Fluorinated polyimides                | 2.3-2.8             | SOD/CVD                        |
|                           | Fluoro-polymers                       | 1.8-2.2             | SOD/CVD                        |
|                           | F-doped amorphous C                   | 2.0-2.5             | CVD                            |
| Inorganic/Organic Hybrids | Si-O-C hybrid polymers based on organo-silsesquioxanes (e.g. MSQ) | 2.0-3.8             | SOD                            |
| Aerogels (Microporous)    | Porous SiO₂ (with tiny free space regions) | 1.2-1.8             | SOD                            |
| Air bridge                |                                       | 1.0-1.2             |                                 |

• All of these approaches are beginning to appear in advanced process flows today.