Exam #2 — EE 531

Winter 2005

This is a take-home exam. You are welcome to use any notes and/or books. However, you are not permitted to have the assistance of any other person on the exam. If you have any questions regarding interpretation of the questions, you should submit your question to class EPost web site.

Your exam papers are due back in my office (EE 218) by 3pm on Thursday, March 17. Please do not spend more than 10 hours actively working on the exam. In completing these questions, feel free to make reasonable assumptions, but be sure to state them clearly and check them when possible. Assume $T = 300\text{K}$ unless otherwise specified.

1. Design the doping versus depth in a PMOS transistor with a p^+ poly gate ($E_f = E_v$) and $t_{ox} =$ 2nm such that it has a long-channel threshold voltage of $-0.4\,\text{V}$ and a subthreshold slope of $75\,\text{mV/decade}$.

   Compare your design to an otherwise identical transistor with constant substrate doping and the same threshold voltage:

   (a) Which has lower off current? Explain.

   (b) Which has higher on (saturation) current? Explain.

   (c) Which device has the lower drain to body junction capacitance? Explain.

   (d) Which transistor will be more immune to reductions in threshold voltage due to short channel effects? Explain.

2. Consider an NMOS transistor with n^+ poly gate, $t_{ox} = 2.5\,nm$ and uniform channel doping. Assuming that long-channel V_T is to be held to 0.5V, determine the minimum channel length and associated substrate doping to keep $I_{\text{off}}/W < 10^{-4} A/\mu\text{m}$ with $V_{GS} = 0\text{V}$ and $V_{DS} = 1.5\text{V}$. Use the simple expression for short channel effects on threshold voltage given in Taur and Ning.

3. An MOS transistor with $t_{ox} = 1.5\,\text{nm}$, a uniform substrate doping of $N_d = 5 \times 10^{18}\text{cm}^{-3}$, and $V_{fb} = 1.0\,\text{V}$ is biased in inversion such that $Q'_I = 8 \times 10^{-7}\ \text{C/cm}^2$. Assume $V_{DS} = V_{BS} = 0$.

   (a) If the p-type poly doping is $5 \times 10^{19}\text{cm}^{-3}$, what gate capacitance would be measured? You can use Eq. 4.58 in Taur and Ning to determine effective thickness of inversion layer (include quantum effects).

   (b) What is the applied gate bias (V_{GS})? Include the increased voltage drop across silicon required due to confinement of inversion layer (Eq. 4.56).

4. Tensile biaxial stress lowers the heavy-hole band relative to the light-hole band (ignore split-off or spin-orbit band). Assume that for an MOS device fabricated in strained Si on relaxed SiGe, this shift is equal to 30meV.

   (a) Calculate the resulting effective mass tensor for the valence band.

   (b) Estimate the change in τ_m for both heavy and light holes assuming elastic isotropic scattering both within and between bands.

   (c) Combine your results to calculate resulting change in the hole mobility.