Homework #5 - EE 531

due 5/21/09

1. Using the structure of the first Sentaurus-Device MOSFET example:

   (a) Based on the simulation results, estimate V_T, m (extract two values, one from saturation voltage and the other from subthreshold slope in the absence of interface states), and $\mu C_{ox}/L$ (current is given per micron of width). Compare these values to calculations based on equations discussed in class.

   (b) If we consider a transistor to be off when $I_{ds} < 10^{-6} A/\mu\text{m}$, calculate the gate voltage required to turn off the gate and compare to simulation results with $V_{ds} = 0.1\,\text{V}$ and $V_{ds} = 2\,\text{V}$.

   (c) Modify and run these files to display a plot of the electron potential versus lateral distance from source to drain in the silicon very close to the Si/SiO_2 interface for the MOSFET biased in the cutoff, linear and saturation regimes. Comment on the results with respect to the barrier(s) seen by electrons in flowing from the source to the drain.

   (d) For the same bias conditions, plot the electrical potential as a function of depth (vertical distance) at $L/10$ (near source), $L/2$ and $9L/10$ (near the drain). Compare the voltages dropped across the silicon and the oxide to models used in class to predict MOSFET behavior.

   (e) On a 2D plot, view the electric field vector in the silicon under the same conditions as in (a). Is the gradual channel approximation a good one throughout the device? If not, where is it violated?

   (f) Analyze GIDL and channel avalanche breakdown by calculating substrate current as a function of V_{DS} for $V_{SB} = 0$ and $V_{GS} = -0.5,\ 0,\ 0.5,\ 2.0\,\text{V}$.

2. Assuming that the dependence of the channel mobility on the vertical electric field is given by

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \alpha \bar{\mathcal{E}}_{\text{vert}} \mu_0},$$

   where $\bar{\mathcal{E}}_{\text{vert}}$ is the average of the vertical electric field at the Si-SiO_2 interface (depends on Q'_s) and just below the inversion layer (depends on Q'_d), determine an expression for the effective mobility as a function of $(V_{GS} - V_T)$, V_{SB} and V_{CS}. Is this model equivalent to any of the options provided with Sentaurus-Device (see manual)? If so which one(s) and under what condition(s)?

3. Problem 3.8 in text.

4. You are told by your process engineers that they can control doping concentration within $\pm 5\%$ and channel dimensions within $\pm 0.02\mu\text{m}$.

   (a) Given these process variations, design an NMOS transistor with an n^+ poly gate ($\phi_{poly} \cong \chi_s$), 4nm thick oxide, deep source/drains, a very shallow threshold-shifting implant, and otherwise constant substrate doping to minimize the worst-case switching time under the constraint that the worst-case off-state leakage current is less than 1nA/μm (with $V_{GS} = 0$V and including DIBL). Assume that the power supply voltage is 2V (set to limit gate field to 5MV/cm) and that the switching speed can be approximated by

$$W\left[4LC'_{ox} + (0.5\mu\text{m})C'_j\right] V_{dd}/I_{DS},$$

   (C'_j is junction capacitance for S and D) where I_{DS} is calculated from Eq. 3.76 for $V_{GS} = V_{DS} = 2V$ and $V_{SB} = 0$. You have control over the substrate doping, implant dose (to shift V_T, ignore effect on mobility), and channel dimensions L and W. Use Eq. 3.66 in the text for short channel effects and DIBL and the model for channel length modulation from Eq. 3.97 (use $\mathcal{E}_{sat} = 2\mathcal{E}_c$, $v_{sat} = 8 \times 10^6$ cm/s). Use value of effective mobility calculated at the source.

(b) Test your design using Medici (remember to use worst-case analysis). You can modify the example used in previous homework. Suggest possible reasons for significant discrepancies. Test the switching speed first by just determining I_{DS}. Then use an output load consisting of a capacitor equal to $4WLC'_{ox}$ (fan-out of 4 equivalent transistors) in a transient simulation. Initialize the capacitor with a voltage equal to 2V and determine the time to discharge down to 0.5 V (roughly V_T).

5. Briefly describe (1-2 paragraphs) your plans for final project.